WHAT IS CLAIMED IS:

1. A digital control variable delay circuit comprising:

n amplitude control units which are connected in parallel and each of which receives a pair of input clock signals to be supplied to a differential pair and receives m-bit digital control signals, n and m each indicating a natural number of 2 or larger; and

waveform shaping unit which is shared between the n amplitude control units and is connected, in common, to the outputs of the n amplitude control units, wherein

the respective pairs of clock signals supplied to the n amplitude control units are shifted in phase by about 1/n period,

each amplitude control unit being capable of varying the amplitude of each of the pair of clock signals into (m + 1) values using the m-bit digital control signals, and outputting a pair of amplitude-varied clock signals,

the waveform shaping unit receiving a pair of added clock signals obtained by adding and combining the pairs of amplitude-varied clock signals outputted from the n amplitude control units, shaping the waveform of each of the pair of added clock signals, and then outputting a pair of resultant clock signals as output signals.

2. The digital control variable delay circuit according to Claim 1, wherein

each amplitude contr l unit comprises a pair of MOS

transistors sharing a common terminal and constituting a differential pair, m current source circuits connected in parallel, and a pair of load resistors connected to respective output terminals of the pair of MOS transistors,

the m current source circuits each comprising a current source and a switching unit, each current source and the corresponding switching unit being connected in series, each of the switching units being turned on or off by the corresponding one of the m-bit digital control signals,

one end of each of the m current source circuits connected in parallel being connected to ground and the other end thereof being connected to the common terminal of the pair of MOS transistors,

the output terminals of the pair of MOS transistors outputting the pair of amplitude-varied clock signals.

3. The digital control variable delay circuit according to Claim 2, wherein in each of the n amplitude control units, the m switching units are turned on and off in response to the respective m-bit digital control signals to vary the number of current sources connected to the pair of MOS transistors so as to change current flowing through the pair of load resistors, thus varying the amplitude of each of the pair of clock signals into (m + 1) values.

4. The digital control variable delay circuit according to Claim 3, wherein in each of the n amplitude control units, when all of the m-bit digital control

signals are turned off, the amplitude of each of the pair of amplitude-varied clock signals indicates zero.

5. The digital control variable delay circuit according to Claim 3, wherein in each of the n amplitude control units, when one or more of the m-bit digital control signals are turned on, the amplitude of each of the pair of amplitude-varied clock signals lies in a range of (the maximum value × 1/m) to (the maximum value × m/m).

6. The digital control variable delay circuit according to Claim 5, wherein in each of the n amplitude control units, when all of the m-bit digital control signals are turned on, each of the pair of amplitude-varied clock signals has the maximum amplitude.

7. The digital control variable delay circuit according to Claim 2, wherein in each of the n amplitude control units, the size ratio in the m current sources is set so as to generate no delay variations after phase interpolation in the whole digital control variable delay circuit and is set so that (m + 1) digital control signals of (n × m) digital control signals are temporarily turned on in the whole digital control variable delay circuit.

8. The digital control variable delay circuit according to Claim 7, wher in the size ratio in the m current sources is set on the basis of the current ratio in the m current sources.